Journal of Artificial Intelligence and Data Mining (JAIDM), Vol. 12, No. 1, 2024, 15-25.

Shahrood University of Technology

Journal of Artificial Intelligence and Data Mining (JAIDM)
Journal homepage: http://jad.shahroodut.ac.ir

Research paper

Low-order Robust Controller for DC-DC Quadratic Buck Converter: Design and Implementation

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Article Info

Article History:
Received 10 September 2023
Revised 12 January 2024
Accepted 24 January 2024

DOI:10.22044/jadm.2024.13584.2475

Keywords:
Quadratic Buck Converter, μ Synthesis, Order Reduction, Robust Controller, Optimization.

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Abstract

This paper addresses a key challenge in designing a suitable controller for DC-DC converters to regulate the output voltage effectively within a limited time frame. In addition to non-minimum phase behavior of such type of converter, a significant issue, namely parametric uncertainty, can further complicate this task. Robust control theory is an efficient approach to deal with this problem. However, its implementation often requires high-order controllers, which may not be practical due to hardware and computational constraints. Here, we propose a low-order robust controller satisfying the robust stability and performance criteria of conventional high-order controllers. To tackle this issue, a constraint optimization problem is formulated, and the evolutionary algorithms are adopted to achieve the optimal parameter values of the controller. Both simulation and experimental outcomes have been documented, and a comparative analysis with an optimal Proportional-Integral (PI) controller has been conducted to substantiate efficiency to the proposed methodology.

1. Introduction

Recently, the extensive utilization of DC-DC converters in various applications such as DC microgrids, storage batteries, wind turbines, photovoltaic systems, and LED lamp drivers has promoted to the exploration of different converter topologies including step-down and step-up configurations [1-7]. These converters exhibit non-linear behavior with a time-varying structure due to their switching operation, making it challenging to achieve satisfactory performance using conventional linear methods over a wide range of operation [8]. Consequently, the design of controllers for these converters has garnered significant interest, with researchers employing diverse control techniques to regulate voltage. Several studies have been documented in the literature, encompassing approaches such as the Kharitonov theorem [9, 10], fuzzy logic control [11-15], fractional control [16, 17], linear-quadratic regulator (LQR) [18, 19], adaptive backstepping control [20-22], sliding mode control techniques [23-26], and feedback linearization control [27].

The objectives of system performance and voltage regulation objectives are affected by parameter perturbations stemming from uncertainties. Consequently, it becomes imperative to address these uncertainties to meet performance and stability criteria [28]. Robust control theory has emerged as a widely recognized methodology to achieve these objectives. μ-synthesis is a key technique for designing a robust controller that utilizes the structured singular value (SSV). Through this method, two goals involving robust stability (RS) and robust performance (RP) can be guaranteed against different types of uncertainties [29]. A linearized model of the system is required to design a controller using this approach. For representing the performance specifications of the closed-loop system and shaping the exogenous signals, multiple weighting functions may be included. This has been method confirmed to

provide much better performance than conventional controllers [30]. The DK iteration algorithm has emerged as the predominant approach for addressing the μ-synthesis problem in conventional methods. However, this approach yields a controller with a high-order, which could pose challenges for real-time implementation due to constraints imposed by hardware and computational capabilities.

Additionally, it should be noted that in certain scenarios, this algorithm has the potential to converge towards local minima [31]. A systematic procedure to avoid high-order controllers is to reduce the order of controller through model order reduction. However, this reduction can often degrade robustness criteria and system performance [32]. One potential approach to address the previously mentioned problems involves the utilization of a fixed-structure robust controller. This method offers a practical and lower-order controller to effectively implement the system [33, 34]. To acquire the parameters for the low-order controller, a constraint optimization problem is proposed, and heuristic algorithms employed to solve it. These algorithms have garnered significant attention in their advancement [34, 36]. [37] Used Particle Swarm Optimization (PSO) to obtain parameters of low-order controller designed based on the Kharitonov approach for a buck converter with an order of two and no zero or pole situated on the right-half plane. Besides advantages of this method, it should be mentioned that the complexity to determine acceptable bounds for the parameters of the controller significantly increases if the order of the system or controller grows.

Among step-down DC-DC converters, the Quadratic Buck Converter (QBC) has the ability to reduce the level of input voltage considerably. The main contribution of this article is to design a low-order robust controller for a DC-DC QBC converter, which suffers from uncertainties in its parameters. The validity of the designed controller is verified by conducting a comparative analysis with two widely used methods: the DK iteration method, which is a conventional approach for addressing the μ-synthesis problem, and an optimal PI controller. Simulations illustrate the appropriate behaviour of the proposed control algorithm for voltage regulation. The difference in order between the proposed controller and the resultant controller by DK iteration provides a simplicity to implementation on a Micro Controller Unit (MCU).

The remainder of this article is structured as what follows. In Section 2, an extracted small signal averaged model of the converter is presented, followed by the discussion of approaches for designing a robust controller. Sections 3 and 4 detail simulations and the experiments, respectively. The last section provides conclusions regarding key aspects and remarks.

2. Problem Formulation

In this section, the design of a robust controller based on μ synthesis is discussed. The conventional method for solving an optimization problem to obtain a robust controller leads to a high-order controller. This makes it difficult to implement in practice. The proposed robust fixed-structure controller based on μ can be a suitable solution to avoid high-order counterpart, which maintains the feature of the resultant controller by DK iteration beside its considerable low order. In this section, first, the system description of the DC-DC quadratic buck converter is presented, and preliminaries of the designed controller are described in section B. Then the proposed method to the low-order controller is studied.

2.1. System description

The quadratic buck converter is equivalent to two conventional buck converters arranged in cascade, featuring only a single active and three passive switches. This converter comprises two inductors and two capacitors, making it a fourth-order system. The conversion ratio in Continuous Conduction Mode (CCM) is determined by the following equation:

$$\frac{V_o}{V_{in}} = D^2 \tag{1}$$

In comparison with a conventional buck converter, a quadratic buck offers a wider conversion ratio and can achieve lower voltage at the same duty cycle. Prior to designing a controller, it is essential to establish a dynamic model for the converter. The average model techniques, as outlined in [38], have been employed to derive the dynamic equations of the converter. This approach is widely used for modeling power electronic circuits in both continuous and discontinuous conduction modes [39]. As shown in the topology of the circuit in Figure 1(a), there are two low-pass filters: L_1 and C_1 in the first stage, L_2 and C_2 in the second stage. The variables of the QBC are the voltage of capacitors and the current of inductors. In CCM, QBC works in two operation modes, as depicted in Figures 1(a) and 1(b). The first mode is active when the switch is on. In this stage, diodes D_1 and D_3 are open, and D_2 is conducting. The capacitors C_1 and C_2 are charged and discharged, respectively, and

the inductor L1 is charged by source E. The state-space equation of this operation mode is described by Eq. (2). In the second mode, when the switch is off, diodes D_1 and D_3 are on, and D_2 is off.

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ \frac{1}{C_2} & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} E \tag{2}$$

In this stage, capacitors are charged by inductors. The state-space equation related to this mode is given by:

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} E \tag{3}$$

By integrating Eqs. (2) and (3), the average non-linear equation of the QBC is extracted as:

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{D}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} E \tag{4}$$

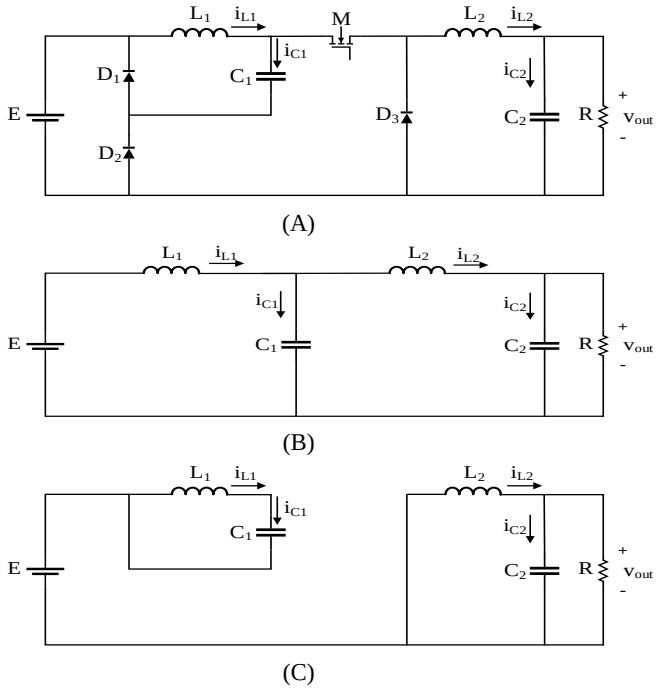


Figure 1. (A) Quadratic buck converter circuit topology, (B) The switch is on, (C) The switch is off.

The equilibrium point of the converter in the nominal situation is given by:

$$V_{C1e} = ED,\ V_{C2e} = ED^2,\ I_{L1e} = \frac{ED^3}{R},\ I_{L2e} = \frac{ED^2}{R} \tag{5}$$

Considering the small perturbations in all steady-state variables and the duty cycle of the QBC, the small signal model is derived as:

$$\begin{bmatrix} \dot{\tilde{i}}_{L_1} \\ \dot{\tilde{i}}_{L_2} \\ \dot{\tilde{v}}_{C_1} \\ \dot{\tilde{v}}_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & \frac{D}{L_1} & \frac{-1}{L_2} \\ \frac{1}{C_1} & \frac{-D}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} \tilde{i}_{L_1} \\ \tilde{i}_{L_2} \\ \tilde{v}_{C_1} \\ \tilde{v}_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{E}{L_1} \\ \frac{V_{C1e}}{L_2} \\ -\frac{I_{L2e}}{C_1} \\ 0 \end{bmatrix} \tilde{d} \tag{6}$$

Where E denotes the input voltage, $\tilde{d}$ corresponds to the control signal of the converter, which takes a valid range of [0, 1], and R represents the load resistance. The output voltage corresponds to the capacitor voltage in the second stage is $V_{c2e} = V_o$. The small signal transfer function from control signal (duty cycle) to output voltage is derived by applying Laplace transform, which is represented as [40]:

$$T_{QBC} = \frac{\tilde{v}_o}{\tilde{d}} = \frac{V_{C2e}}{DC_2L_2} \times \frac{s^2 + a_1 s + a_0}{s^4 + b_1 s^3 + b_2 s^2 + b_3 s + b_4} \tag{7}$$

Where:

$$b_0 = \frac{1}{L_1C_1L_2C_2},\ b_1 = \frac{1}{RC_2},\ b_2 = \frac{D^2}{C_1L_2} + \frac{1}{L_2C_2} + \frac{1}{L_1C_1}$$
$$b_3 = \frac{D^2}{RC_1L_2C_2} + \frac{1}{RL_1C_1C_2},\ a_1 = -\frac{D^2}{RC_1},\ a_0 = \frac{2}{L_1C_1} \tag{8}$$

It is apparent that the transfer function (7) has two zeros, which are located in the right-half plane (RHP). This imposes a critical limitation on bandwidth, and satisfactory performance will be difficult to achieve. The nominal values and the range of uncertainty on the circuit's parameters are listed in Table 1.

2.2 Preliminaries

A common representation of a closed-loop system experiencing uncertainties and external inputs can be visualized through an interconnected system, as demonstrated in Figure 2. Within the present conceptual framework, exogenous inputs including reference signals, noise, and disturbances are represented as "*w*", while the output error, which involves the control actions, tracking errors, and the regular output, is denoted by "*z*". The known component of the system, comprising the nominal plant and weighting functions, is represented by "*P*", with "*K*" referring to the controller. The

uncertainty set is visually depicted by "Δ". Additionally, the input and output signals associated with the dynamic uncertainties are designated as "*v*" and "*d*", respectively. The general framework in Figure 2 can be simplified by a lower linear fractional transformation of *P* and *K*, $M(P,K) = F_l(P,K)$, as is shown in Figure 3.

Table 1. Parameters of the quadratic buck converter.

Parameter	Nominal value	Range of uncertainty
R	5Ω	[-20% , 20%]
L_1	470µ	[-30% , 30%]
L_2	330µ	[-30% , 30%]
C_1	33µ	[-30% , 30%]
C_2	100µ	[-30% , 30%]
E	12v	[8 ~ 16]
f_{sw}	62.5kHz	-

In this structure, the closed-loop system is influenced by exogenous inputs and uncertainties. According to the concept of structured singular value (μ), the closed-loop stability of a system can be determined. The system is considered robustly stable if and only if it is internally stable, and the maximum upper structured singular value of the first component of the matrix *M* is less than unity [41].

$$\mu_{\Delta}(M_{11}) < 1 \tag{9}$$

The tool employs a robust performance analysis approach by incorporating a fictitious uncertainty block, denoted by Δ_F, which encompasses the system's performance specifications. Blocks Δ_F and Δ are merged and converted to $\tilde{\Delta}$, as seen in Figure 4. Based on the given configuration, the closed-loop system is considered to have robust performance if the condition described by Equation (10) is satisfied.

$$\mu_{\tilde{\Delta}}(M) < 1 \tag{10}$$

The common technique for solving the μ synthesis problem is the *DK* iteration approach. This converter comprises two inductors and two capacitors, making it a fourth-order system. In each stage, an H_∞ optimization problem is solved for a fixed given matrix *D* to get controller *K*. Subsequently, the controller is set and a convex optimization problem is solved within a specified frequency range to determine *D*. This iterative process continues until the maximum structured singular value of the closed-loop system is reduced below unity. However, there are two main limitations associated with this method. Firstly, there is a risk of the algorithm converging to local minima. Secondly, it may result in the generation of a high-order controller that is noticeable in the system.

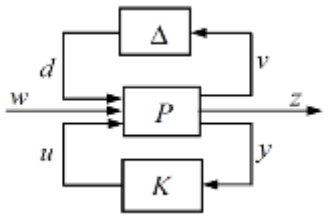


Figure 2. General framework [38].

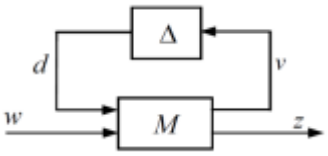


Figure 3. Robust stability analysis [38].

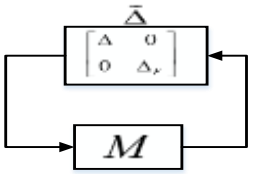


Figure 4. Robust performance analysis [38].

2.3 Proposed method

In order to address the challenges associated with the high-order controller resulting from the *DK* iteration method, this section proposes a solution in the form of a constraint optimization method. By this approach, one can select the arbitrary low-order control structure, while the resultant controller satisfies the robust conditions described by (9) and (10), even though, it can carry the characteristics of the high-order controller. The proposed method to avoid the high-order controller is a constraint optimization problem such that the resultant controller satisfies both robust stability and robust performance conditions, while its order is dramatically lower than the controller by the *DK* method. Generally, a known simple structure is selected for the controller as low-order as possible, and the controller's parameters are determined through evolutionary algorithms for solving the pre-defined optimization problem. In this manuscript, we present the subsequent optimization problem.

$$\begin{aligned} &\min_{K(s)} \left\| M(s) \right\|_{\mu} \\ &\text{such that: } \left\| M_{11}(s) \right\|_{\mu} < 1 \end{aligned} \tag{11}$$

In this context, the robust stability (9) is formulated as a constraint optimization, while the robust performance condition (10) is regarded as the fitness function.

3. Simulation Results

Besides the non-minimum phase behavior of the converter, another challenging issue is the existence of uncertainty in the parameters of the circuit, which poses difficulties in regulating the output voltage. To account for model uncertainty, the multiplicative uncertainty description given by equation (12) is employed. Figure 5 illustrates the closed-loop system with uncertainty.

$$P = (1 + \Delta W) T_{QBC} \tag{12}$$

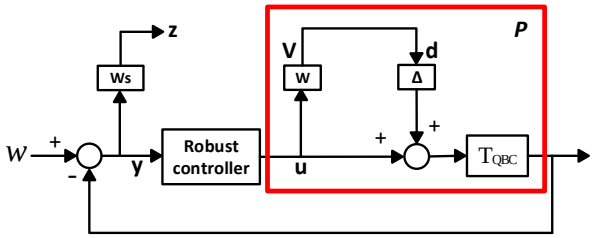


Figure 5. Block diagram of closed-loop uncertain system.

In Figure 5, W, W_s, and Δ represent the weighting function, the performance function, and the unknown perturbation, respectively. It is considered that Δ is a norm-bounded, where its infinity norm is smaller than or equal to unity. Through multiplicative uncertainty description and the determination of its maximum value, it can be proven that W is greater than any relative model mismatch across all frequency ranges. Figure 6 demonstrates the behavior of multiplicative uncertainty and the corresponding weighting function. Equations (13) and (14) describe the weighting and the performance functions, respectively.

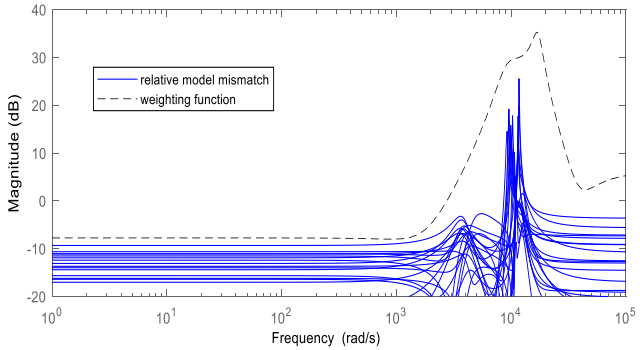


Figure 6. Relative model mismatch and weighting function.

Equation (15) describes the controller through the *DK* iteration. As can be seen, the resulting controller has an order 17, posing challenges for both analog implementation using op-amps or digital implementation on microcontrollers.

$$W_s = \frac{0.1\,s + 478}{1.283\,s + 4.78\times10^{-5}} \tag{13}$$

$$W = \frac{2.028s^4 + 4.742\times10^4 s^3 + 3.18\times10^9 s^2 + 6.901\times10^{12} s + 1.032\times10^{16}}{s^4 + 8105 s^3 + 3.963\times10^8 s^2 + 1.667\times10^{12} s + 2.514\times10^{16}} \tag{14}$$

$$K_{DK} = \frac{N_1 N_2}{D_1 D_2} \tag{15}$$

Where:

$$N_1 = 2134.8(s^2 + 2832s + 4.347\times10^6)(s^2 + 5179s + 1.041\times10^7)$$
$$(s^2 + 1796s + 1.312\times10^7)(s^2 + 1849s + 1.921\times10^7)$$
$$N_2 = (s^2 + 4653s + 8.521\times10^7)(s^2 - 3559s + 1.573\times10^8)$$
$$(s^2 + 3452s + 2.95\times10^8)(s^2 + 2.475\times10^4 s + 5.599\times10^8)$$
$$D_1 = (s + 3.726\times10^{-5})(s^2 + 2705s + 4.22\times10^6)(s^2 + 5241s + 9.978\times10^6)$$
$$(s^2 + 3680s + 7.392\times10^6)(s^2 + 1808s + 1.361\times10^7)$$
$$D_2 = (s^2 + 2521s + 1.498\times10^8)(s^2 + 2.247\times10^4 s + 6.205\times10^8)$$
$$(s^2 + 5.965\times10^4 s + 2.131\times10^9)(s^2 + 2.111\times10^4 s + 1.508\times10^9)$$

To avoid the high-order controller, we apply he proposed method, which formulates a constraint optimization problem to ensure that the resulting controller satisfies both robust stability and robust performance conditions. Additionally, the order of controller is significantly lower compared to the controller obtained through the *DK* method. In this method, a specified structure is chosen for the controller, and evolutionary algorithms are adopted to determine the parameters of the controller. The optimization constraint is based on robust stability using μ, with robust performance considered as the cost function. In this study, for a more comprehensive comparison, three well-known optimization algorithms, namely ant bee colony (ABC), genetic algorithm (GA), and particle swarm optimization (PSO) [42], are utilized. The proposed structure for the low-order controller is described in Equation (16) with four parameters. The range of values for each parameter is listed in Table 2.

$$K_{proposed} = \frac{as + b}{s^2 + cs + d} \tag{16}$$

Table 2. Search space of the parameters of controller.

Parameter	a	b	c	d
Range	[0 ~ 100]	[0 ~ 1e5]	[0 ~ 1e3]	[0 ~ 1]

The number of iteration of all algorithms is set to 100. Figure 7 shows the convergence rate of the cost function for PSO, GA, and ABC, respectively. For better evaluation, the controller that has been synthesized by *DK* iteration is reduced by the Hankel norm to the same order with the proposed structure. All low-order controller parameters are listed in Table 3. Robust stability and performance of the robust controllers based on μ analysis are

represented in Figures 8 and 9, respectively. As can be seen, the proposed controller, designed using three algorithms, satisfies both robust conditions. However, the reduced-order controller, determined by the Hankel norm and having the same order as the proposed controller, does not meet the criteria for robust stability and performance, as illustrated in Figure 10.

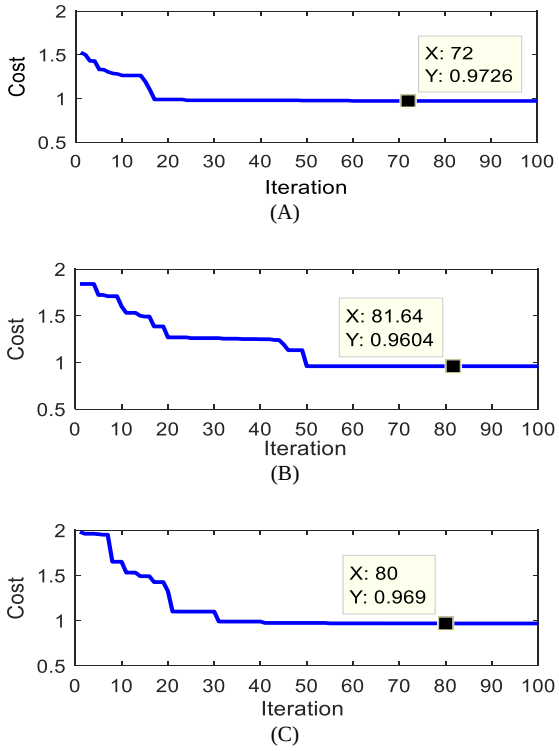


Figure 7. Convergence of cost function by algorithms. A) ABC, B) GA, C) PSO.

Table 3. Parameters of the low-order proposed controller.

Method	Parameters			
	a	b	c	d
PSO	0.06102	9.312e4	2157	0.05483
GA	0.05603	9.213e4	2106.5	0.01734
ABC	0.05534	9.3916e4	2201.67	0.05407
Hankel	-88.59	7.179e4	1692	0.06301

The maximum structured singular values for the robust stability and performance, for all controllers under discussion are summarized in Table 4. It is readily that a better stability and performance margin is reached by the proposed method in comparison with *DK* iteration, so the proposed controller could inherit the behavior of a robust high-order controller besides has a more simple structure. To validate the controllers, each controller is put on a non-linear physical model of a circuit in the Simulink environment. To more comparison between the proposed controller and the high-order controller, the PI controller is designed whose parameters are extracted by PSO algorithms.

Table 4. Maximum SSV for RS and RP of controllers.

Method	RS	RP
PSO	0.8832	0.9690
ABC	0.8819	0.9726
GA	0.8746	0.9604
DK	0.8945	0.9770
Hankel	13.1062	13.9470

The cost function for this optimization problem is based on integral absolute error (IAE). The structure of PI controller is as:

$$C = K_p(1+\frac{1}{K_i s}) \tag{17}$$

Where:

$$K_p = 0.0343 \qquad K_i = 9.385929\times10^{-4} \tag{18}$$

In simulation, different scenarios are executed. Initially, all circuit parameters are set to their nominal values. Subsequently, the impact of set point changes is examined. Following that, the system's performance is investigated under variations in the resistance load. The circuit is then subjected to the worst-case scenario, considering uncertainties. Figure 11 illustrates the output voltage regulation at the desired 5V for all controllers. As observed, there is a nearly identical transient response for all the proposed low-order controllers. However, the parameters that have been obtained by GA provides a quicker response compared to others by PSO and ABC algorithms. Moreover, the proposed controllers not only meet the robustness criterion and maintain the performance of high-order robust controllers but also have a better response. This observation is particularly significant, indicating that the approach for deriving low-order controllers is more practical. Additionally, it facilitates the implementation of controller coding in the C language for microcontroller.

In the following, the parameters extracted by GA are considered as the proposed controllers and compare with the conventional *DK* iteration and PI. The ability to track the set point changing of controllers is shown in Figure 12. The desired output voltage is changed to 6V at t = 0.02 s, and then it is switched to 3.3V at t = 0.04. It is obvious that the robust controllers can track various voltage levels properly without oscillation and faster than PI. In the next step, the effect of uncertainty on the resistance load is analyzed. In this scenario, the resistive load is changed from 4 to 6 at t = 0.02 s, and the output response is illustrated in Figure 13. It can be seen that the robust controllers return faster the output voltage to the initial state after a step change in the load and the output experiences smaller overshoot in comparison with PI.

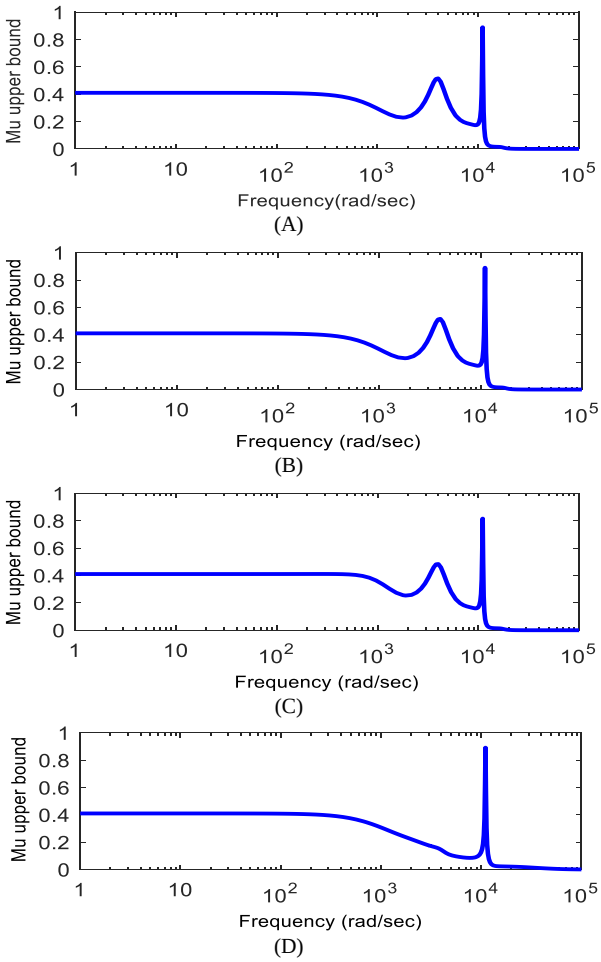
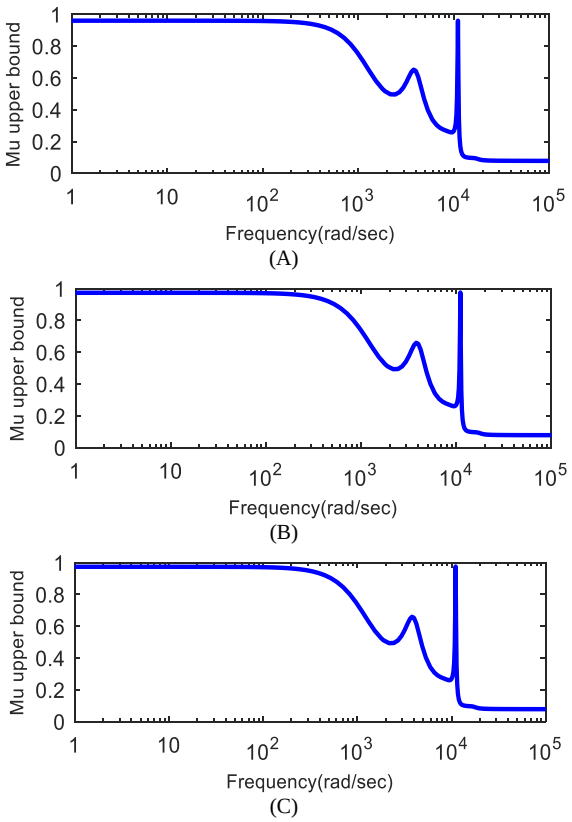


Figure 8. Robust stability analysis based on μ. A) ABC, B) GA, C) PSO, D) DK.



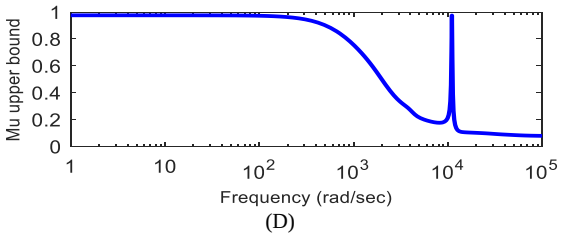


Figure 9. Robust performance analysis based on μ. A) ABC, B) GA, C) PSO, D) *DK*.

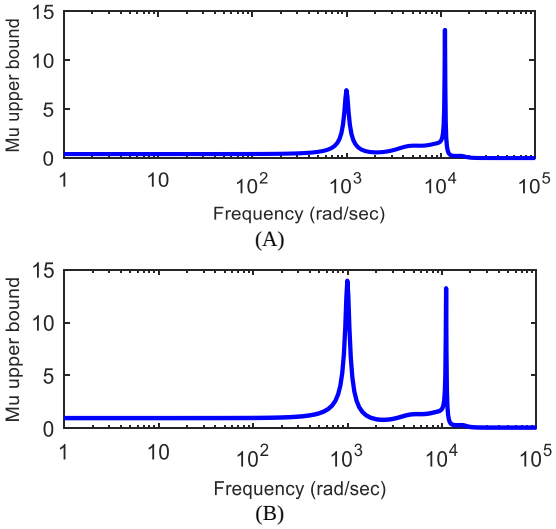


Figure 10. Robust stability and performance analysis based on from reduced-order by Hankel. A) robust stability, B) robust performance.

In terms of uncertainty, the converter is considered with the worst-case when parameters of the converter are deviated from their nominal values as follows:

$$R = 6\Omega \quad L_1 = 329\mu H \quad L_2 = 429\mu H$$
$$C_1 = 23.1\mu F \quad C_2 = 130\mu F \quad E = 16v \tag{19}$$

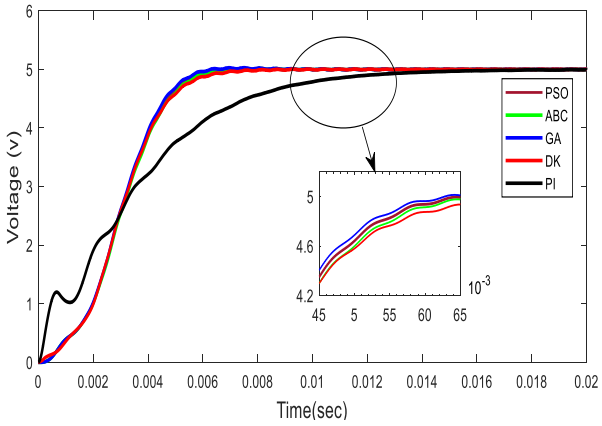


Figure 11. Output voltage for nominal situation.

Figure 14 depicts the output voltage under the worst-case situation, and the proposed controller behavior shows an acceptable response to output voltage regulation. Totally, it concludes that the proposed controller can realize proper characteristics of the resultant high-order controller

by powerful *DK* iteration tool while the difference order between them is considerable.

4. Experimental Results

In this section, the effectiveness of the proposed robust controller is investigated. The first step involves discretization of the controller, which has been carried out using Tustin's method with sample time 100 us. For the unit controller, a STM32F103RET6 is used.

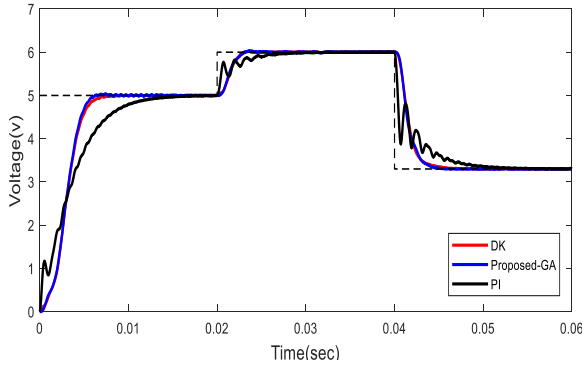


Figure 12. Reference tracking.

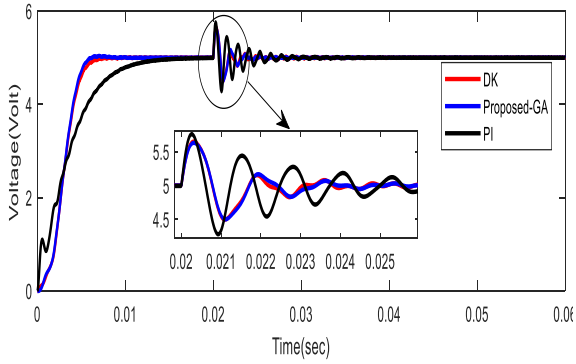


Figure 13. Resistance load changing.

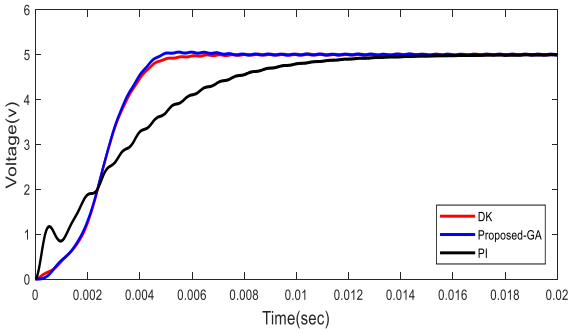


Figure 14. Output voltage for worst case situation.

To generate the PWM control signal for hardware QBC, a sawtooth signal with 62.5 kHz frequency is compared with the extracted signal from the controller's equation, and, therefore, an appropriated square signal is generated. The hardware schematic of the quadratic buck converter is shown in Figure 15 including the power stage, the control unit, the DC power supply, and the oscilloscope card. The power unit involves a Mosfet IRF540 and IR2104 as switch and gate driver, respectively.

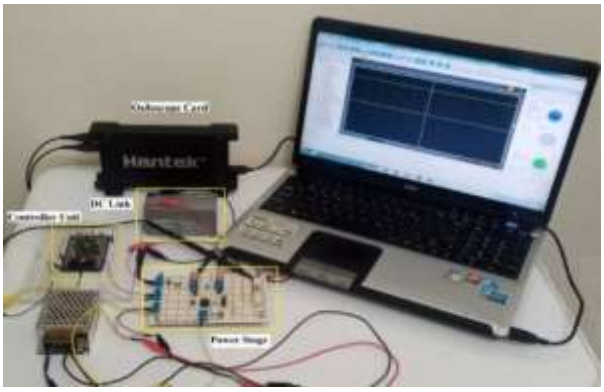
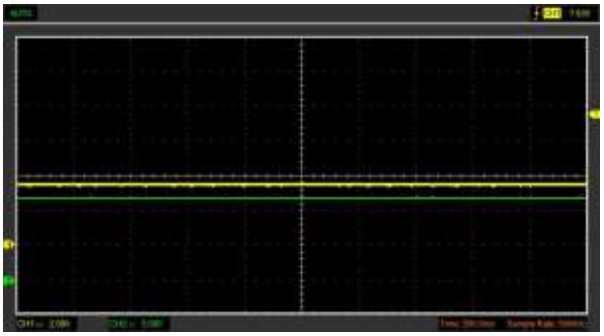
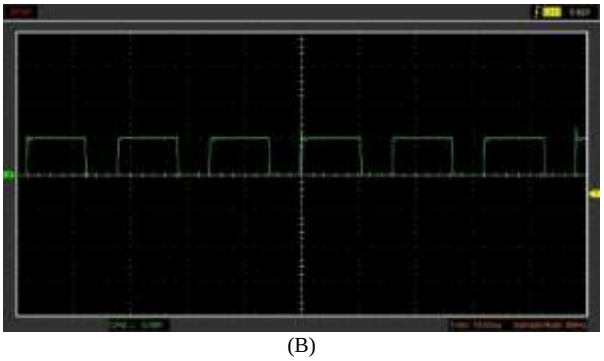


Figure 15. Experimental set-up.

The output voltage of the converter and control signal for different voltage levels are illustrated in Figures 16 and 17. In Figure 16(a) and 17(A), the input voltage source (CH2) is 12V, and the output voltage (CH1) for voltage levels are 3.3 V and 5 V, respectively. The related PWM signal produced by the controller to trigger the Mosfet for desired voltage is shown in Figures 16(b) and 17(b).



(A)



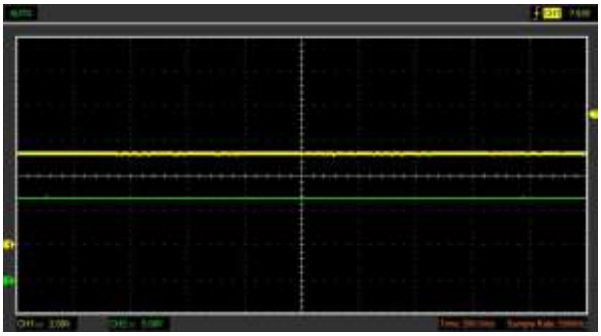
(B)

Figure 16. Set point 3.3V. (A) Output voltage, (B) Control signal.

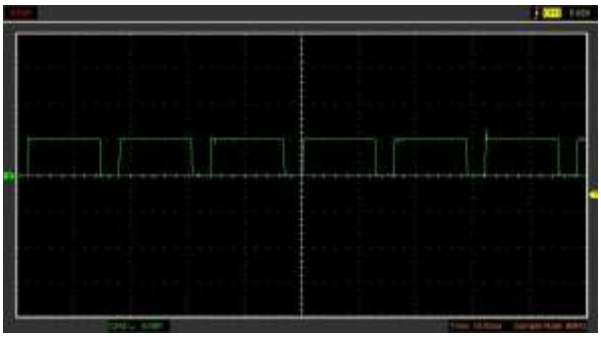
5. Conclusion

In this paper, a robust low-order controller with a simple structure for a quadratic buck converter is proposed. Evolutionary algorithms have been employed to determine the parameters of the proposed controller by solving a predefined constraint optimization problem. The genetic

algorithm exhibits superior performance in terms of stability and performance margin based on μ. Unlike the model order reduction Hankel method, this controller has carried properly the characteristics of the robust high-order controller by conventional *DK* approach without any degradation of the system performance. In comparison with PSO-based PI controller, the proposed controller has better convergence to reference voltage, and smaller recovery time in the situation of parameters changing. Thanks to the proposed controller's low-order structure, it is more convenient to implement on the Microcontroller unit controller. Simulation and experimental results confirmed the ability of the proposed robust low-order controller to maintain output voltage on desired levels.



(A)



(B)

Figure 17. Set point 5 V. (A) Output voltage, (B) Control signal.

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کنترل‌کننده مقاوم مرتبه پایین برای مبدل باک درجه دوم DC-DC: طراحی و ساخت

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ارسال ۲۰۲۳/۰۹/۱۰؛ بازنگری ۲۰۲۳/۰۱/۱۲؛ پذیرش ۲۰۲۳/۰۱/۲۴

چکیده:

این مقاله به یک چالش کلیدی در طراحی کنترل‌کننده مناسب برای مبدل‌های DC-DC به منظور تنظیم موثر ولتاژ خروجی در یک بازه زمانی محدود می‌پردازد. علاوه بر نامینیمم فاز بودن این نوع مبدل، مسئله مهم، یعنی عدم قطعیت پارامتری، این کار را پیچیده تر کند. نظریه کنترل مقاوم یک رویکرد موثر برای مقابله با این مشکل است. با این حال، اجرای آن اغلب به کنترل‌کننده‌هایی با مرتبه بالا منجر می‌شود که ممکن است به دلیل محدودیت‌های سخت‌افزاری و محاسباتی عملی نباشد. در این مقاله، یک کنترل کننده مقاوم درجه پایین پیشنهاد می‌شود که معیارهای پایداری مقاوم و عملکرد مقاوم کنترل کننده های معمولی مرتبه بالا را برآورده می‌سازد. بدین منظور، یک مسئله بهینه‌سازی مقید فرمول‌بندی می‌شود و الگوریتم‌های تکاملی برای دستیابی به مقادیر بهینه پارامترهای کنترل‌کننده استفاده می‌شوند. نتایج شبیه‌سازی و عملی گزارش می‌شوند و یک تحلیل مقایسه‌ای با کنترل‌کننده بهینه PI برای اثبات کارایی روش پیشنهادی انجام می‌شود.

کلمات کلیدی: مبدل باک درجه دوم، سنتز μ، کاهش مرتبه، کنترل کننده مقاوم، بهینه‌سازی.